ABSTRACT

A scheduling circuit of the present invention includes an IP (Internet Protocol) scheduling/format converting section for scheduling input IP packets and converting each of them to ATM (Asynchronous Transfer Mode) cells. The IP scheduling/format converting section includes a plurality of packet FIFOs (First-In First-Out memories). The ATM cells output from each packet FIFO are written to corresponding one of a plurality of cell FIFOs. An ATM scheduling section schedules the ATM cells received from each cell FIFO cell by cell.